SCHOTTKY BIPOLAR LSI MICROCOMPUTER SET

The INTEL Bipolar Microcomputer Set is a family of Schottky bipolar LSI circuits which simplify the construction of microprogrammed central processors and device controllers. These processors and controllers are truly microprogrammed in the sense that their control logic is organized around a separate read-only memory called the microprogram memory. Control signals for the various processing elements are generated by the microinstructions contained in the microprogram memory. In the implementation of a typical central processor, as shown below, the microprogram interprets a higher level of instructions called macroinstructions, similar to those found in a small computer. For device controllers, the microprograms directly implement the required control functions.

3003 LOOK-AHEAD CARRY GENERATOR

The INTEL 3003 Look-Ahead Carry Generator (LCG) is a high speed circuit capable of anticipating a carry across a full 16-bit 3002 Central Processing Array. When used with a larger 3002 CP Array multiple 3003 carry generators provide high speed carry look-ahead capability for any word length.

The LCG accepts eight pairs of active high cascade inputs (X,Y) and an active low carry input and generates active low carries for up to eight groups of binary adders.

High Performance – 10 ns typical propagation delay

Compatible with INTEL 3001 MCU and 3002 CPE

DTL and TTL compatible

Full look-ahead across 8 adders

Low voltage diode input clamp

Expandable

28-pin DIP

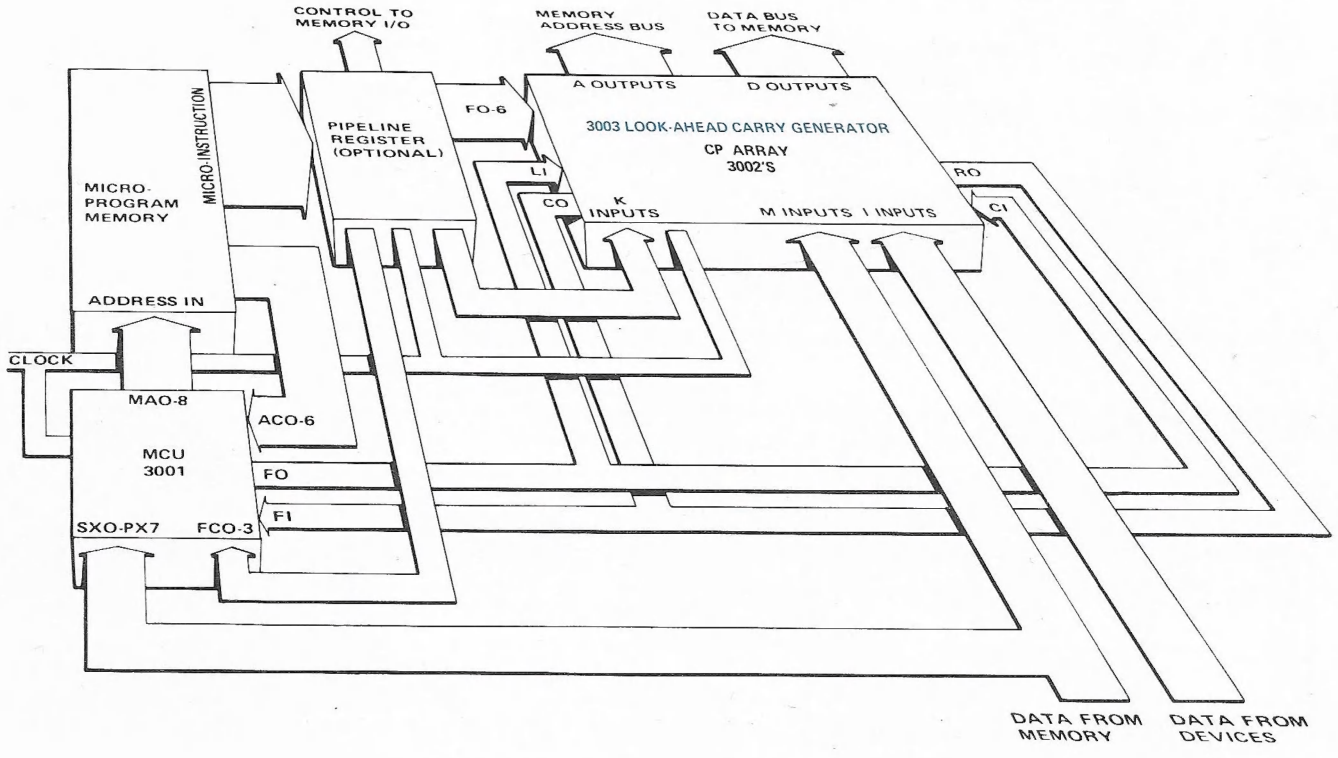
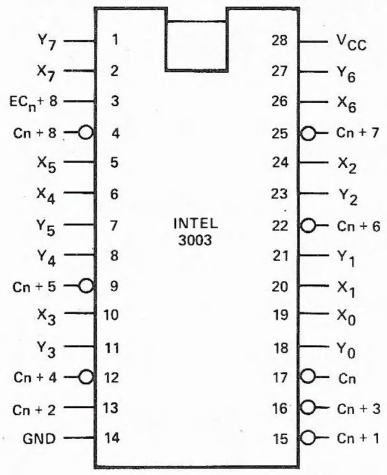


Diagram of a Typical System

Other members of the INTEL Bipolar Microcomputer Set:

3001 Microprogram Control Unit
3002 Central Processing Element
3212 Multi-Mode Latch Buffer
3214 Priority Interrupt Control Unit
3226 Inverting Bi-Directional Bus Driver
3301A Schottky Bipolar ROM (256 x 4)
3304A Schottky Bipolar ROM (512 x 8)
3601 Schottky Bipolar PROM (256 x 4)
3604 Schottky Bipolar PROM (512 x 8)

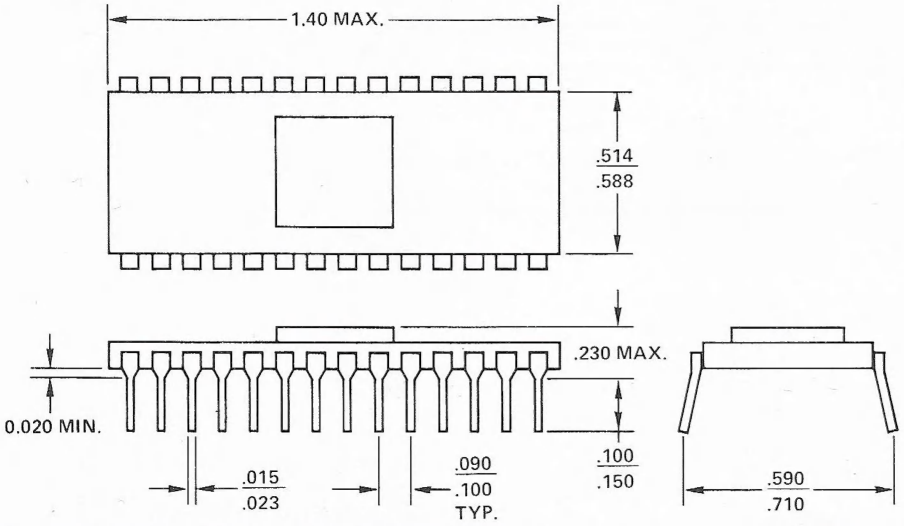
PACKAGE CONFIGURATION



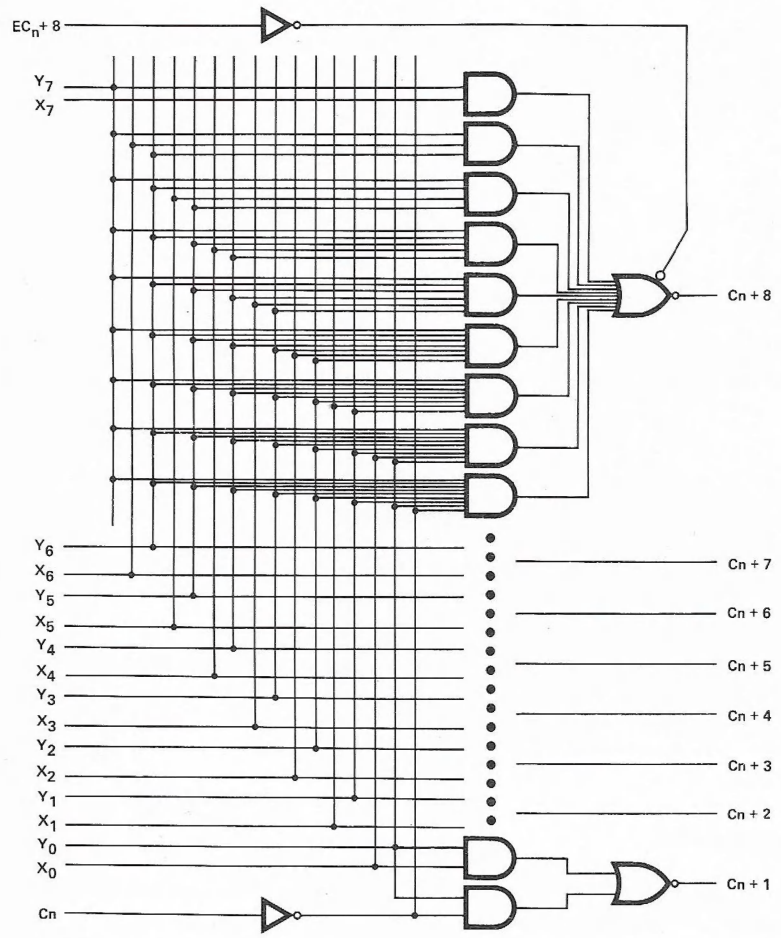
PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1,7,8,11,18 21,23,27	Y_0-Y_7	Standard carry look-ahead inputs	Active HIGH
2,5,6,10,19 20,24,26	X_0-X_7	Standard carry look-ahead inputs	Active HIGH
17	C_n	Carry input	Active LOW
4,9,12,13,15 16,22,25	C_{n+1}-C_{n+8}	Carry outputs	Active LOW
3	EC_{n+8}	C_{n+8} carry output enable	Active LOW
28	V_{CC}	+5 volt supply	
14	GND	Ground	

PACKAGE OUTLINE



3003 LOGIC DIAGRAM



3003 LOGIC EQUATIONS

The 3003 Look-Ahead Generator is implemented in a compatible form for direct connection to the 3001 MCU and 3002 CPE. Logic equations for the 3003 are:

$$\overline{C_n + 1} = Y_0X_0 + Y_0\overline{C}_n$$

$$\overline{C_n + 2} = Y_1X_1 + Y_1Y_0X_0 + Y_1Y_0\overline{C}_n$$

$$\overline{C_n + 3} = Y_2X_2 + Y_2Y_1X_1 + Y_2Y_1Y_0X_0 + Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_n + 4} = Y_3X_3 + Y_3Y_2X_2 + Y_3Y_2Y_1X_1 + Y_3Y_2Y_1Y_0X_0 + Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_n + 5} = Y_4X_4 + Y_4Y_3X_3 + Y_4Y_3Y_2X_2 + Y_4Y_3Y_2Y_1X_1 + Y_4Y_3Y_2Y_1Y_0X_0 + Y_4Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_n + 6} = Y_5X_5 + Y_5Y_4X_4 + Y_5Y_4Y_3X_3 + Y_5Y_4Y_3Y_2X_2 + Y_5Y_4Y_3Y_2Y_1X_1 + Y_5Y_4Y_3Y_2Y_1Y_0X_0 + Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_n + 7} = Y_6X_6 + Y_6Y_5X_5 + Y_6Y_5Y_4X_4 + Y_6Y_5Y_4Y_3X_3 + Y_6Y_5Y_4Y_3Y_2X_2 + Y_6Y_5Y_4Y_3Y_3Y_1Y_0X_0 + Y_6Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n$$

$\overline{C_n + 8}$ = High Impedance State when $EC_n + 8$ Low

$$\overline{C_n + 8} = Y_7X_7 + Y_7Y_6X_6 + Y_7Y_6Y_5X_5 + Y_7Y_6Y_5Y_4X_4 + Y_7Y_6Y_5Y_4Y_3X_3 + Y_7Y_6Y_5Y_4Y_3Y_2X_2 + Y_7Y_6Y_5Y_4Y_3Y_2Y_1X_1 + Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0X_0 + Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n \text{ when } EC_n + 8 \text{ high}$$

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Current	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

T_A = 0°C to +70°C

SYMBOL	PARAMETER	TYP.(1)	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		V	V_{CC} = 4.75V, I_C = -5 mA
I_F	Input Load Current:			
	C_n and EC_n + 8	-0.07	mA	V_{CC} = 5.25V, V_F = 0.45V
	All Other Inputs	-0.9	mA	
I_R	Input Leakage Current:			
	C_n and EC_n + 8		μA	V_{CC} = 5.25V, V_R = 5.25V
	All Other Inputs		μA	
V_{IL}	Input Low Voltage		V	V_{CC} = 5.0V
V_{IH}	Input High Voltage		V	V_{CC} = 5.0V
I_{CC}	Power Supply Current	80	mA	V_{CC} = 5.25V, All Y + EC_n + 8 high, All X + C_n low
V_{OL}	Output Low Voltage (All Output Pins)	0.35	V	V_{CC} = 4.75V, I_{OL} = 5 mA
V_{OH}	Output High Voltage (All Output Pins)	3	V	V_{CC} = 4.75V, I_{OH} = -1 mA
I_{OS}	Short Circuit Output Current (All Output Pins)	40	mA	V_{CC} = 5V
$I_{O(off)}$	Off-State Output Current (C_n + 8)		μA	V_{CC} = 5.25V, V_O = 5.25V

NOTES:
(1)Typical values are for T_A = 25°C and nominal supply voltage

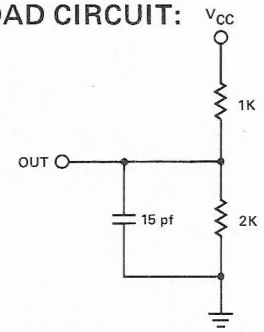
A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$

SYMBOL	PARAMETER	TYP.(1)	UNIT
t_{XC}	X, Y to Outputs	10	ns
t_{CC}	Carry In to Outputs	13	ns
t_{EN}	Enable Time, $C_n + 8$	20	ns

(1) Typical values are for $T_A = 25°C$ and nominal supply voltage.

TEST LOAD CIRCUIT:



TEST CONDITIONS:

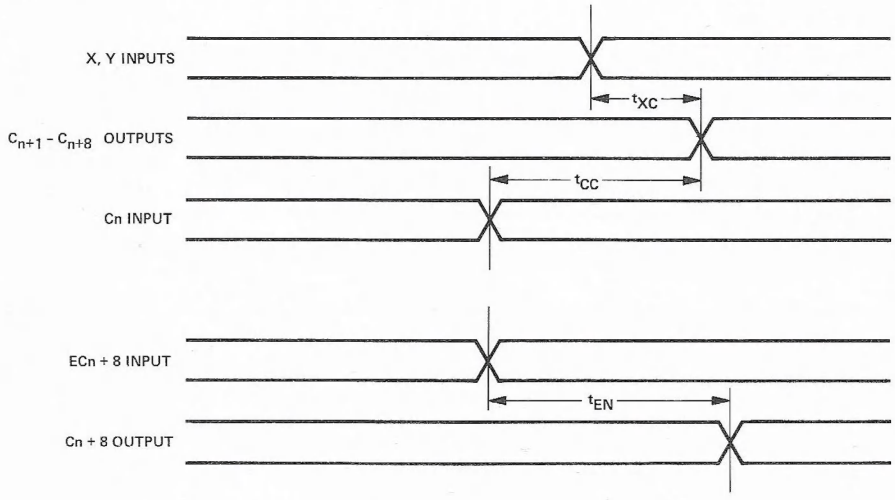
Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

CAPACITANCE(2) $T_A = 25°C$

SYMBOL		PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance	C_n and $EC_n + 8$ inputs				pF
		All other inputs				pF
C_{OUT}	Output Capacitance	$C_n + 8$				pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$ and $T_A = 25°C$.

3003 WAVEFORMS



3003 TYPICAL CONFIGURATIONS

The 3003 LCG can be directly tied to the 3001 MCU and a 3002 CP array of any word length. The following figures represent typical configurations of 16- and 32-bit CP arrays. Figures 1 and 2 illustrate use of the 3003 in a system where the carry output (CO) to the 3001 MCU is rippled through the high order CPE slice. Figure 3 illustrates use of the 3003 in a system where tri-state output C_{n+8} is connected directly to the flag input on the 3001 MCU. C_{n+8} is disabled during shift right by decoding that instruction externally, thus multiplexing C_{n+8} with the shift right (RO) output of the low order CPE slice.

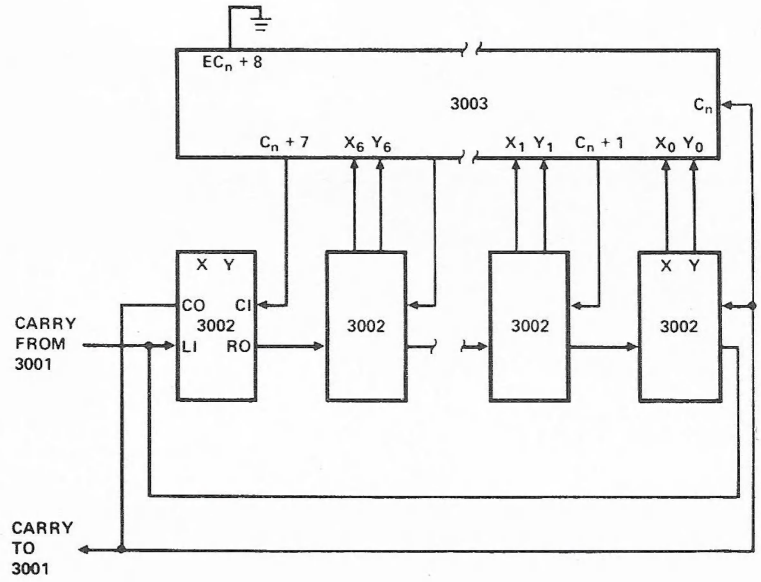


Figure 1. Carry Look-Ahead Configuration with Ripple through the Left Slice (16-Bit Array)

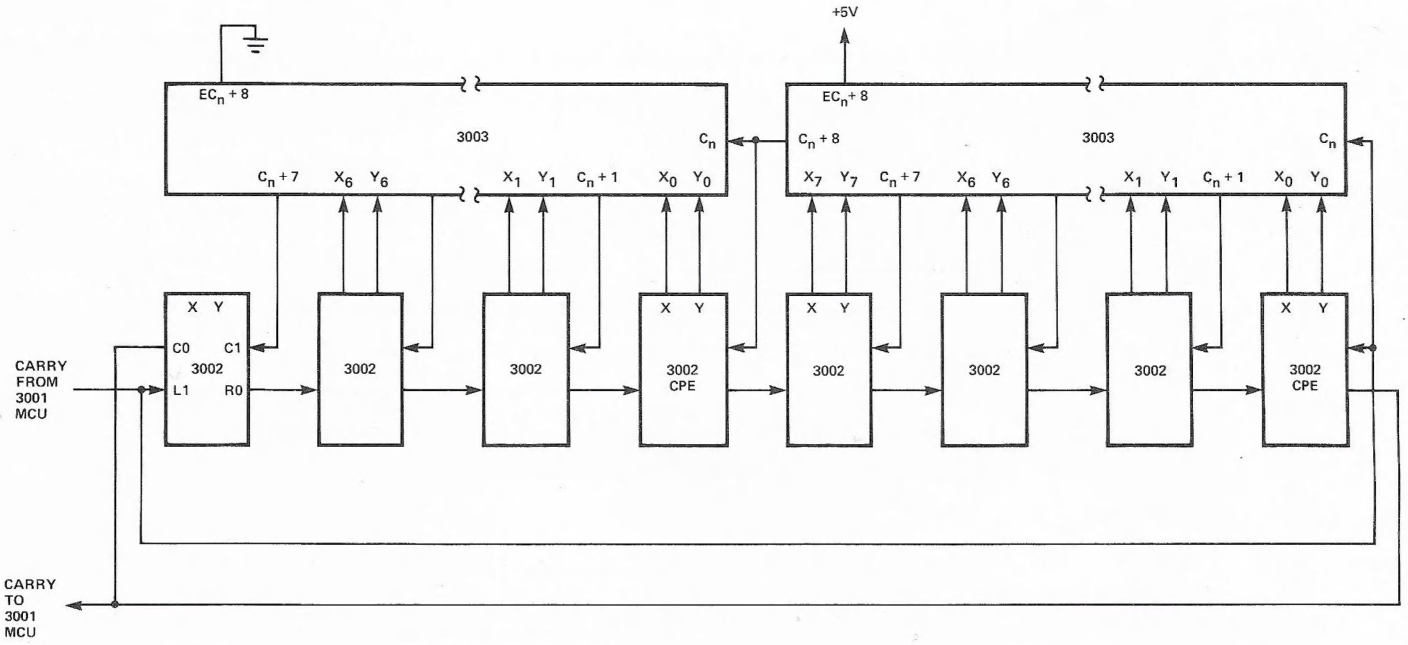


Figure 2. Carry Look-Ahead Configuration with Ripple through the Left Slice (32-Bit Array)

3003 TYPICAL CONFIGURATIONS

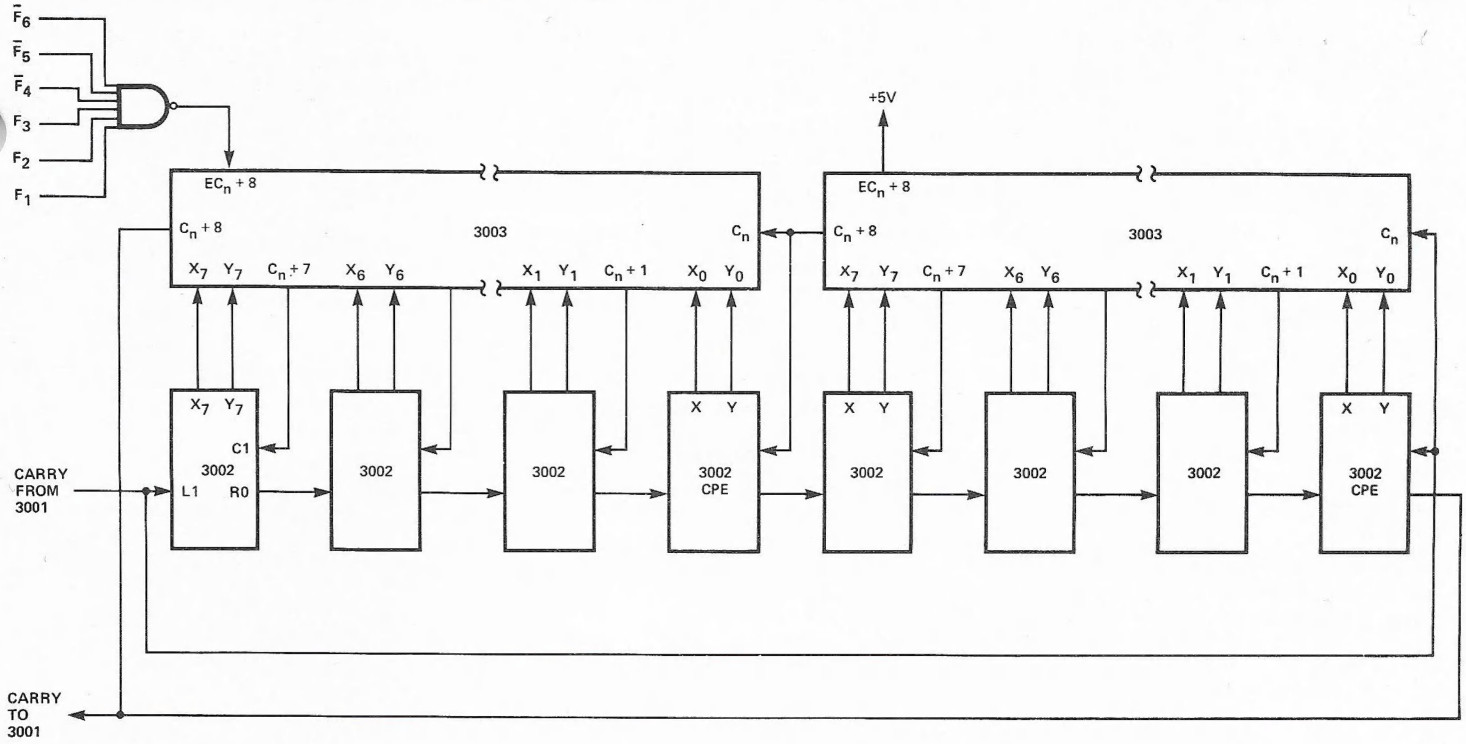


Figure 3. Carry Look-Ahead Configuration with No Carry Ripple through the Last Slice (32-Bit Array)

ORDERING INFORMATION

Part Number	Description
C3003	Look-Ahead Carry Generator

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NOTE: This is a preliminary specification and is subject to revision without notice.

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